What is claimed is:

1. A data system receiving a periodic word clock (WC) signal, comprising:

a phase locked loop (PLL) for receiving said WC signal and generating a first clock having a frequency that is a multiple of said WC signal; and

a clock generator for receiving the first clock and generating a plurality of second clock signals that have frequencies that are submultiples of the first clock signal.

2. The data system of claim 1 wherein said clock generator outputs one of the second clock signals having a same frequency as the WC signal to the PLL, and said PLL adjusts the first clock signal based on the received one of the second clock signals.

3. The data system of claim 1 further including:

a control circuit responsive to the second clock signals for generating control signals.

4. The data system of claim 3 further including:

a storage element responsive to the control signals for outputting all data words in the storage element.

5. The data system of claim 4 further including:

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a multiplexor for passing the output data to a data pin in response to the control signals.

6. The data system of claim 5 wherein said multiplexor outputs the output data based on a single transition of said WC signal.

7. The data system of claim 3 further including:

a storage element responsive to the control signals for receiving data.

8. The data system of claim 1 wherein said PLL and clock generator are incorporated on a single chip.

9. The data system of claim 8 wherein said PLL includes a charge pump.

10. A data system receiving a periodic word clock (WC) signal, comprising:

a transmitter including

a first input for receiving said WC signal,

first means for generating a plurality of clock signals based on the WC signal; and

a first output connected to a transmission line for the transmission of data; and

a receiver including

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a first input for receiving said WC signal;

a second input, connected to said transmission line, for receiving data transmitted by said transmitter; and

second means for generating a plurality of clock signals based on the WC signal.

11. The data system of claim 10 wherein the first means for generating includes:

a phase locked loop (PLL) for receiving said WC signal and generating a first clock having a frequency that is a multiple of said WC signal; and

a clock generator for receiving the first clock and generating a plurality of second clock signals that have frequencies that are submultiples of the first clock signal.

12. The data system of claim 11 wherein said clock generator outputs one of the second clock signals having a same frequency as the WC signal to the PLL, and said PLL adjusts the first clock signal based on the received one of the second clock signals.

13. The data system of claim 11 further including:

a control circuit responsive to the second clock signals for generating control signals.

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14. The data system of claim 13 further including:

a storage element responsive to the control signals for outputting all data words in the storage element.

15. The data system of claim 14 further including:

a multiplexor for passing the output data to a data pin in response to the control signals.

16. The data system of claim 15 wherein said multiplexor outputs the output data based on a single transition of said WC signal.

17. The data system of claim 10 wherein the second means for generating includes:

a phase locked loop (PLL) for receiving said WC signal and generating a first clock having a frequency that is a multiple of said WC signal; and

a clock generator for receiving the first clock and generating a plurality of second clock signals that have frequencies that are submultiples of the first clock signal.

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18. The data system of claim 17 wherein said clock generator outputs one of the second clock signals having a same frequency as the WC signal to the PLL, and said

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PLL adjusts the first clock signal based on the received one of the second clock signals.

19. The data system of claim 17 further including:

a control circuit responsive to the second clock signals for generating control signals.

20. The data system of claim 10 wherein said transmitter is incorporated on a single chip.

21. The data system of claim 20 wherein the transmitter includes a phase locked loop (PLL), said PLL having a charge pump.

22. The data system of claim 10 wherein said receiver is incorporated on a single chip.

23. The data system of claim 22 wherein the receiver includes a phase locked loop (PLL), said PLL having a charge pump.

24. A method for generating clock signals including the steps of:

receiving a word clock (WC) signal;

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generating a first clock having a frequency that is a multiple of said WC signal; and

receiving the first clock and generating a plurality of second clock signals that have frequencies that are submultiples of the first clock signal.

25. The method of claim 24 further including the step of:

generating control signals in response to the second clock signals.

26. The method of claim 24 further including the step of:

initiating the transmission of data words in a storage element based on a single transition of said WC signal.

27. A phase locked loop incorporated on a single chip, said phase locked loop including:

a phase comparator;

a charge pump coupled to an output of the phase comparator; and

a voltage controlled current source coupled to an output of the charge pump.

28. The phase locked loop of claim 27 further including:

a capacitor coupled between an output of the charge pump and ground;

an inverter having an input coupled to the phase comparator;

an on/off current sink coupled to an output of the inverter;

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an on/off current source coupled to the phase comparator and to the on/off current sink; and

a ring oscillator coupled to the output of the on/off current source and the voltage controlled current source.

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